Amendments to the Claims

This Listing of Claims replaces all prior versions, and listings, of claims in this application.

1 – 2 (Cancelled).

3. (Currently Amended) [[A system according to claim 1,]] A system capable of synchronizing clock frequencies of power processing devices and digital signal processing devices, comprising:

a pulse width modulated (PWM) power processing device;

a digital signal processor having a clock capable of generating the digital signal processor operational clock frequency;

where the PWM power processing device is connected to the clock;

where the PWM power processing device uses the clock for its operational clock frequency; and

[[wherein]] where the PWM power processing device includes a [[pulse width modulated]] PWM power supply.

4. (Currently Amended) A system according to claim 3, [[wherein]] where the PWM power processing device provides power to the digital signal processor.

5. (Currently Amended) A system according to claim 3, [[wherein]] where the PWM power processing device further includes a [[pulse width modulated]] PWM power amplifier.

6. (Currently Amended) A system according to claim 5, [[wherein]] where the [[pulse width modulated]] PWM power supply provides power to the [[pulse width modulated]] PWM power amplifier and the PWM digital signal processor.

7. (Currently Amended) A system according to claim [[1]] 3, [[wherein]] where the clock operates at 96kHz.

8. (Currently Amended) A system according to claim 5, [[wherein]] where the [[pulse width modulated]] PWM power amplifier [[drives]] provides power to a loudspeaker.

9. (Currently Amended) [[A system according to claim 1,]] A system capable of synchronizing clock frequencies of power processing devices and digital signal processing devices, comprising:

a pulse width modulated (PWM) power processing device;

a digital signal processor having a clock capable of generating the digital signal processor operational clock frequency;

where the PWM power processing device is connected to the clock;

where the PWM power processing device uses the clock for its operational clock frequency; and

[[wherein]] where the clock has a clock frequency that is used by the digital signal processor.

10. (Currently Amended) A system according to claim 9, [[wherein]] where the digital signal processor uses a multiple of the clock frequency for its operation.

11. (Currently Amended) A system according to claim 9, [[wherein]] where the digital signal processor uses an integer fraction of the clock frequency for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

12. (Currently Amended) A system according to claim 9, [[wherein]] where the digital signal processor uses integer related derivatives of the clock frequency for its operation.

13. (Cancelled).

14. (Currently Amended) [[A system according to claim 13,]] A system for synchronizing clock frequencies of power processing devices and digital signal processing devices, comprising:

a pulse width modulated (PWM) power processing device;

a digital signal processor having a clock capable of generating digital signal processor operational clock frequency;

where the PWM power processing device is connected to the clock;

where the PWM power processing device uses the clock for its operational clock frequency; and

[[wherein]] where the [[pulse width modulated]] PWM power processing device uses a multiple of the clock frequency for its operation.

15. (Currently Amended) [[A system according to claim 13,]] A system for synchronizing clock frequencies of power processing devices and digital signal processing devices, comprising:

a pulse width modulated (PWM) power processing device;

a digital signal processor having a clock capable of generating digital signal processor operational clock frequency;

where the PWM power processing device is connected to the clock;

where the PWM power processing device uses the clock for its operational clock frequency; and

[[wherein the pulse width modulated]] where the PWM power processing device uses an integer fraction of the clock frequency for its operation.

16. (Currently Amended) [[A system according to claim 13,]] A system for synchronizing clock frequencies of power processing devices and digital signal processing devices, comprising:

a pulse width modulated (PWM) power processing device;

a digital signal processor having a clock capable of generating the digital signal processor operational clock frequency;

where the PWM power processing device is connected to the clock;

where the PWM power processing device uses the clock for its operational clock frequency; and

[[wherein the pulse width modulated]] where the PWM power processing device uses integer related derivatives of the clock frequency for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

17. (Currently Amended) A system for synchronizing [[the]] clock frequencies of power processing devices and digital signal processing devices, [[in an electronic system]] comprising:

a pulse width modulated power (PWM) supply;

a [[pulse width modulated]] PWM power amplifier; and

a digital signal processor, including:

[[a clock;]]

[[wherein said]] a clock where the [[pulse width modulated]] PWM power supply is [[communicatively coupled to said]] connected to the clock in [[said]] the digital signal processor;

[[wherein said]] where the [[pulse width modulated]] PWM power amplifier is [[communicatively coupled]] connected to [[said]] the clock in [[said]] the digital signal processor;

[[wherein said]] where the digital signal processor and [[said]] the [[pulse width modulated]] PWM power supply and [[said]] the [[pulse width modulated]] PWM power amplifier use [[said]] the clock in [[said]] the digital signal processor for its operational clock frequency.

18. (Currently Amended) A system according to claim 17, [[wherein]] where the [[pulse width modulated]] PWM power supply provides power to the [[pulse width modulated]] PWM power amplifier and the digital signal processor.

19. (Currently Amended) A system according to claim 17, [[wherein]] where the clock in [[said]] the digital signal processor operates at 96 kHz.

20. (Currently Amended) A system according to claim 17, [[wherein]] where the [[pulse width modulated]] PWM power amplifier [[drives]] provides power to a loudspeaker.

21 - 23 (Cancelled).

24. (Currently Amended) [[A method according to claim 21,]] A method for synchronizing clock frequencies, comprising:

using a clock within a digital signal processor (DSP) to operate the DSP; and

using the clock within the DSP to operate a pulse width modulated (PWM) power processing device; and

[[wherein]] where the PWM power processing device is a PWM power supply.

25. (Currently Amended) A method according to claim 24, [[wherein]] where the PWM power supply provides power to the DSP and to a PWM power amplifier.

26. (Currently Amended) [[A method according to claim 21,]] A method for synchronizing clock frequencies, comprising:

using a clock within a digital signal processor (DSP) to operate the DSP; and

using the clock within the DSP to operate a pulse width modulated (PWM) power processing device; [[wherein]] where the DSP has an input and an output[[;]] and the PWM power [[supply]] processing device has an input and an output.

27. (Currently Amended) A method according to claim 26, [[wherein]] where the output of the DSP feeds the input of the PWM power supply.

28. (Currently Amended) A method according to claim 26, [[wherein]] where the output of the PWM power supply feeds the [[power]] input of the DSP.

29 – 30 (Cancelled).

31. (Currently Amended) [[A method according to claim 21,]] A method for synchronizing clock frequencies, comprising:

using a clock within a digital signal processor (DSP) to operate the DSP; and

using the clock within the DSP to operate a pulse width modulated (PWM) power processing device; and [[wherein]] where the clock has a clock frequency that is used by the DSP.

32. (Cancelled).

33. (Currently Amended) [[A method according to claim 32,]] A method for synchronizing clock frequencies, comprising:

using a clock within a digital signal processor (DSP) to operate the DSP; and

using the clock within the DSP to operate a pulse width modulated (PWM) power processing device, where [[wherein]] the PWM power processing uses a multiple of the clock frequency for its operation.

34. (Currently Amended) [[A method according to claim 31,]] A method for synchronizing clock frequencies, comprising:

using a clock within a digital signal processor (DSP) to operate the DSP; and

using the clock within the DSP to operate a pulse width modulated (PWM) power processing device, where [[wherein]] the DSP uses a multiple of the clock frequency for its operation.

35. (Currently Amended) [[A method according to claim 31,]] A method for synchronizing clock frequencies, comprising:

using a clock within a digital signal processor (DSP) to operate the DSP; and

using the clock within the DSP to operate a pulse width modulated (PWM) power processing device, and where [[wherein]] the clock operates at 96 kHz.

36. (Currently Amended) A system for synchronizing the clock frequencies for an audio electronic device, [[the system]] comprising:

a digital signal processor (DSP) having a clock adapted to provide clock frequency for the operation of the DSP;

a pulse width modulated (PWM) power supply [[communicatively coupled]] operatively connected to the clock in the DSP;

a [[pulse width modulated]] PWM power amplifier [[communicatively coupled]] operatively connected to the clock in the DSP; and

[[wherein]] where the [[pulse width modulated]] PWM power supply and the [[pulse width modulated]] PWM power amplifier use the clock in the DSP for their respective operational clock frequency.

37. (Currently Amended) The system according to claim 36, [[wherein]] where the [[pulse width modulated]] PWM power supply uses an integer multiple or integer fraction of the clock frequency of the clock within the DSP for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

38. (Currently Amended) The system according to claim 36, [[wherein]] where the [[pulse width modulated]] PWM power amplifier uses an integer multiple or integer fraction of the clock frequency of the clock within the DSP for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

39. (New) A system for synchronizing clock frequencies, comprising:

a clock having a clock frequency;

a pulse width modulated (PWM) power processing device for powering a loudspeaker, where the PWM power processing device uses the clock frequency for its operation; and

a digital signal processor that uses the clock frequency for its operation so that the PWM power processing device and the digital signal processor run synchronously.

40. (New) A system according to claim 39, where the clock is inside of the digital signal processor.

41. (New) A system according to claim 39, where the PWM power processing device includes a PWM power supply.

42. (New) A system according to claim 41, where the PWM power processing device provides power to the digital signal processor.

43. (New) A system according to claim 41, where the PWM power processing device includes a PWM power amplifier.

44. (New) A system according to claim 43, where the PWM power supply provides power to the PWM power amplifier and to the digital signal processor.

45. (New) A system according to claim 39, where the clock operates at 96kHz.

46. (New) A system according to claim 39, where the digital signal processor uses a multiple of the clock frequency for its operation.

47. (New) A system according to claim 39, where the digital signal processor uses an integer fraction of the clock frequency for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

48. (New) A system according to claim 39, where the digital signal processor uses integer related derivatives of the clock frequency for its operation.

49. (New) A system according to claim 39, where the PWM power processing device uses a multiple of the clock frequency for its operation.

50. (New) A system according to claim 39, where the PWM power processing device uses an integer fraction of the clock frequency for its operation.

51. (New) A system according to claim 39, where the PWM power processing device uses integer related derivatives of the clock frequency for its operation so that the sum and difference frequencies fall outside of the audible frequency range.